ABSTRACT OF THE DISCLOSURE

A memory cell array is composed of a plurality of blocks separated in column direction every three word lines. Inter-block bit wires are arranged. Each inter-block bit line connects a middle diffusion wire for one of the memory cell units of first block of the separated blocks and the middle diffusion wire for one of the memory cell units of the adjacent second block lying on the other end side of the diffusion wires of the first block. Inter-block ground wires are arranged. Each inter-block ground wire connects the boundary diffusion wire for the one memory cell unit of the first block and the boundary diffusion wire for the one memory cell unit of the adjacent third block lying on the one end side of the diffusion wires of the first block.